

SPV

SimPlus

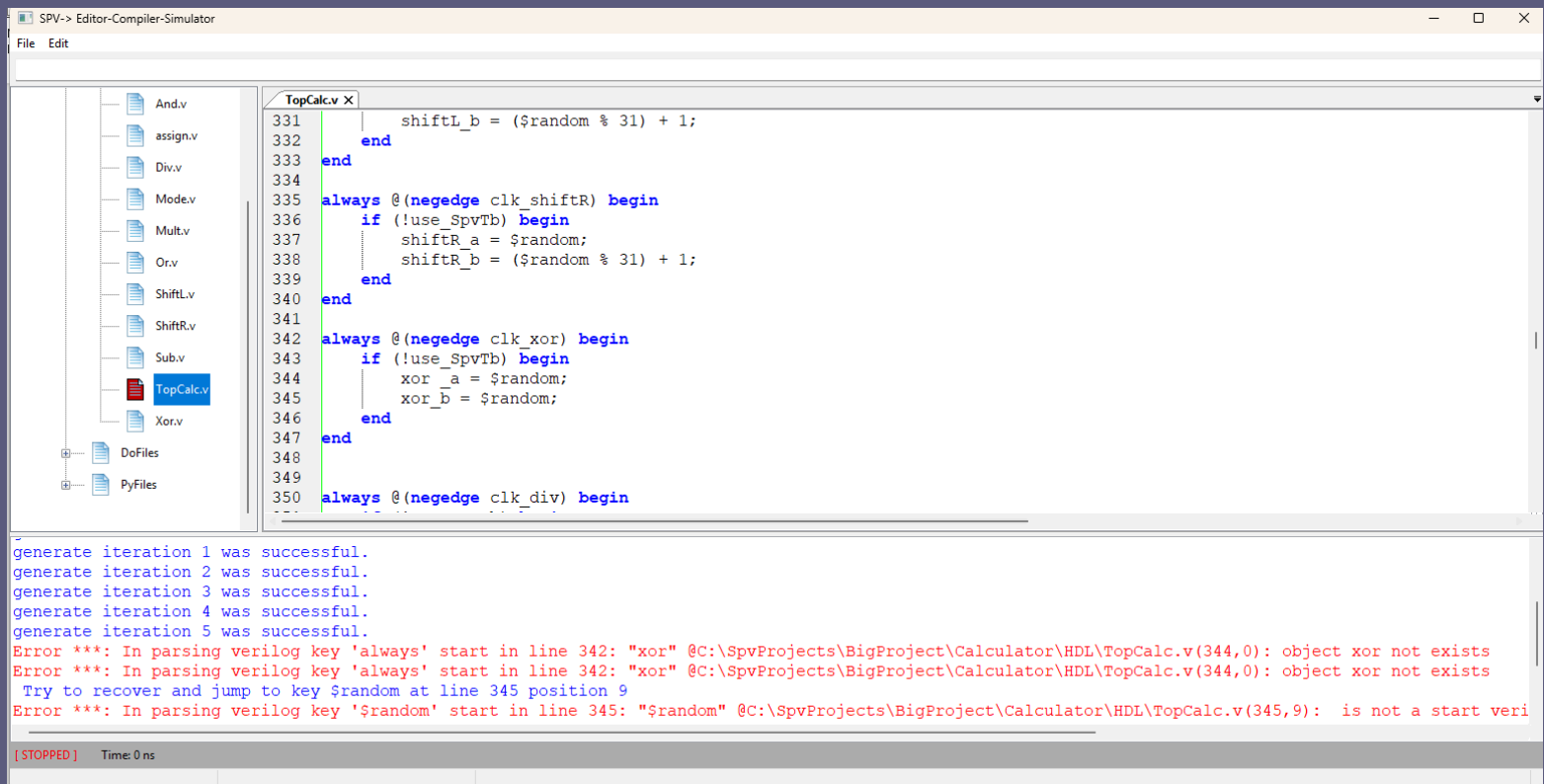


Verification

Integrated Environment for Digital Circuit Design and Verification

Shmuel Amrusi

Verilog Editor & Compilation Environment



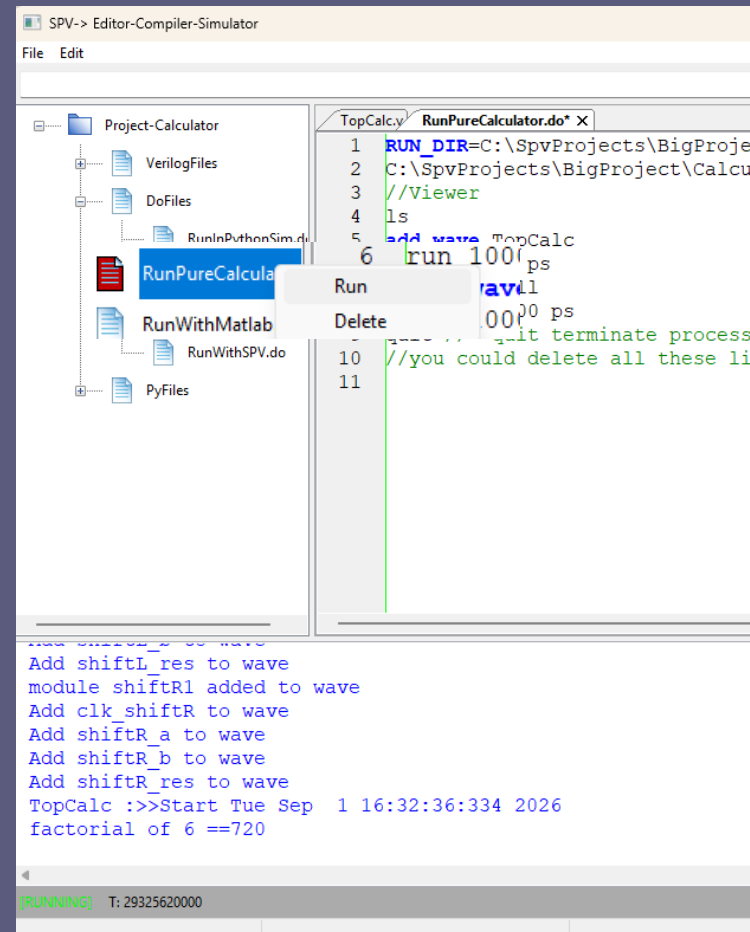
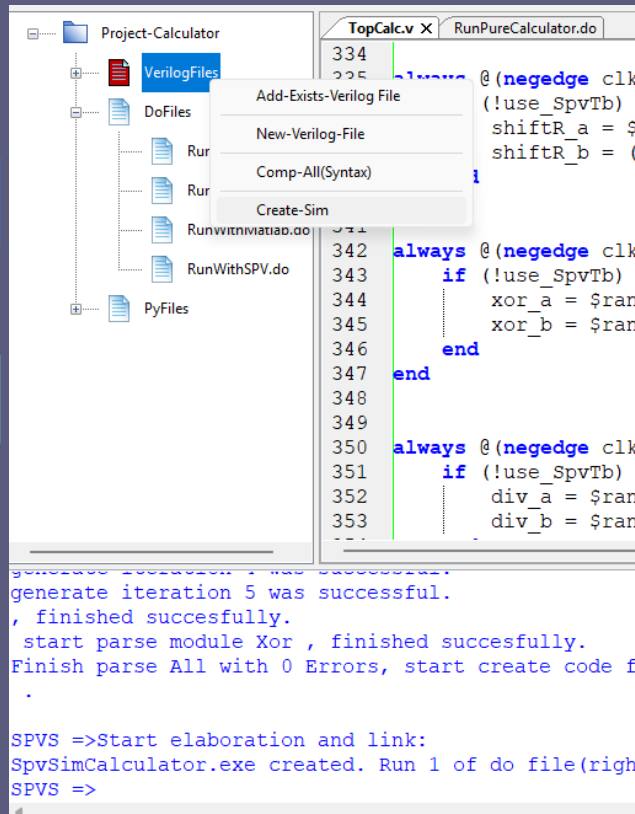
The screenshot displays the SPV Editor-Compiler-Simulator interface. On the left, a file explorer shows a project structure with files like And.v, assign.v, Div.v, Mode.v, Mult.v, Or.v, ShiftL.v, ShiftR.v, Sub.v, TopCalc.v (selected), and Xor.v, along with folders DoFiles and PyFiles. The main editor window shows the content of TopCalc.v, which includes Verilog code for a calculator module. The code defines shift registers and logic for addition, subtraction, multiplication, and division. The bottom panel shows the compilation output, indicating successful iterations and several errors related to parsing Verilog keywords and object references.

```
331      shiftL_b = ($random % 31) + 1;
332  end
333 end
334
335 always @(negedge clk_shiftR) begin
336     if (!use_SpvTb) begin
337         shiftR_a = $random;
338         shiftR_b = ($random % 31) + 1;
339     end
340 end
341
342 always @(negedge clk_xor) begin
343     if (!use_SpvTb) begin
344         xor_a = $random;
345         xor_b = $random;
346     end
347 end
348
349
350 always @(negedge clk_div) begin
```

generate iteration 1 was successful.
generate iteration 2 was successful.
generate iteration 3 was successful.
generate iteration 4 was successful.
generate iteration 5 was successful.
Error ***: In parsing verilog key 'always' start in line 342: "xor" @C:\SpvProjects\BigProject\Calculator\HDL\TopCalc.v(344,0): object xor not exists
Error ***: In parsing verilog key 'always' start in line 342: "xor" @C:\SpvProjects\BigProject\Calculator\HDL\TopCalc.v(344,0): object xor not exists
Try to recover and jump to key \$random at line 345 position 9
Error ***: In parsing verilog key '\$random' start in line 345: "\$random" @C:\SpvProjects\BigProject\Calculator\HDL\TopCalc.v(345,9): is not a start veri

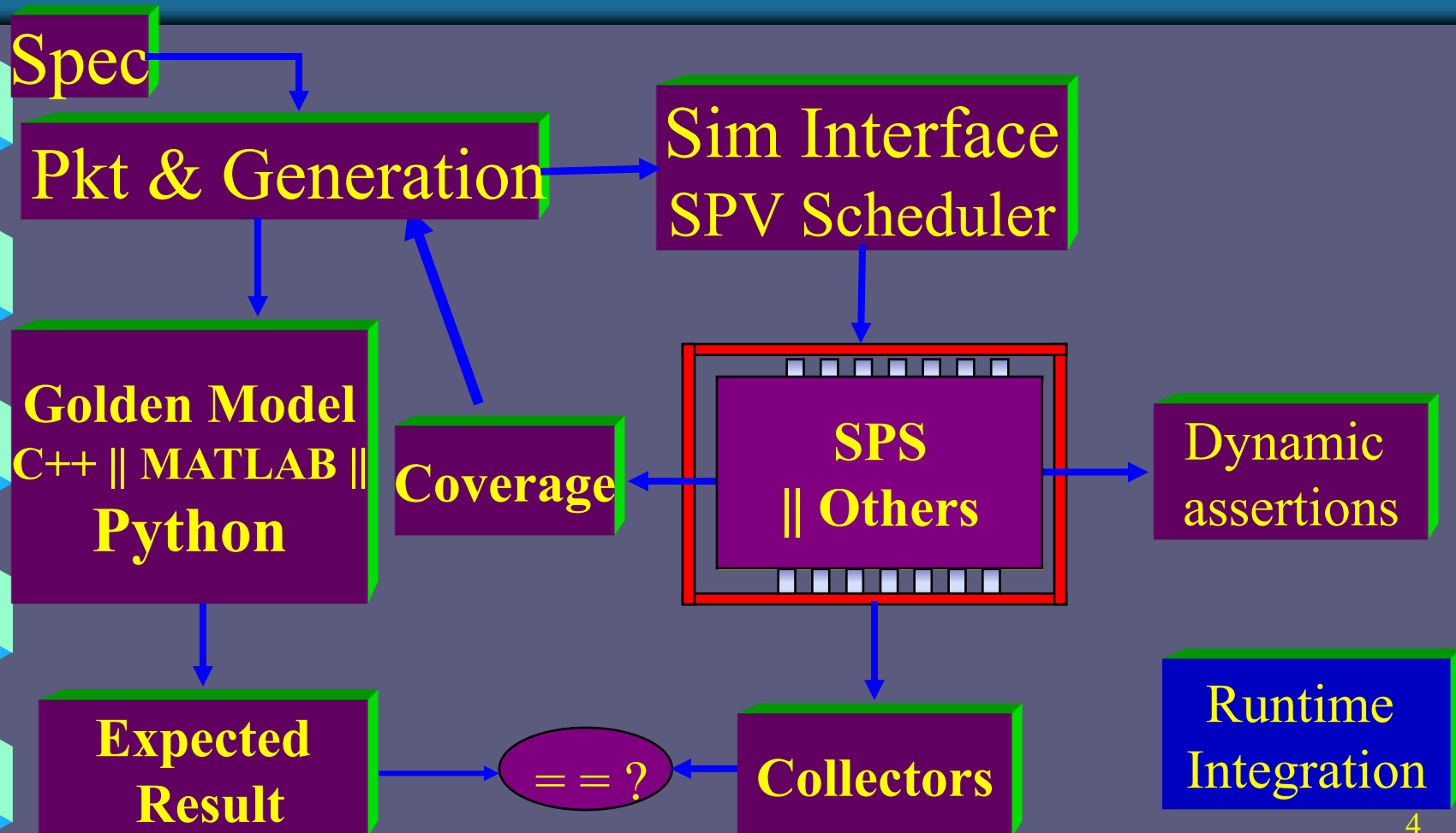
[STOPPED] Time: 0 ns

Unified Workspace for Code, Compilation, and Simulation

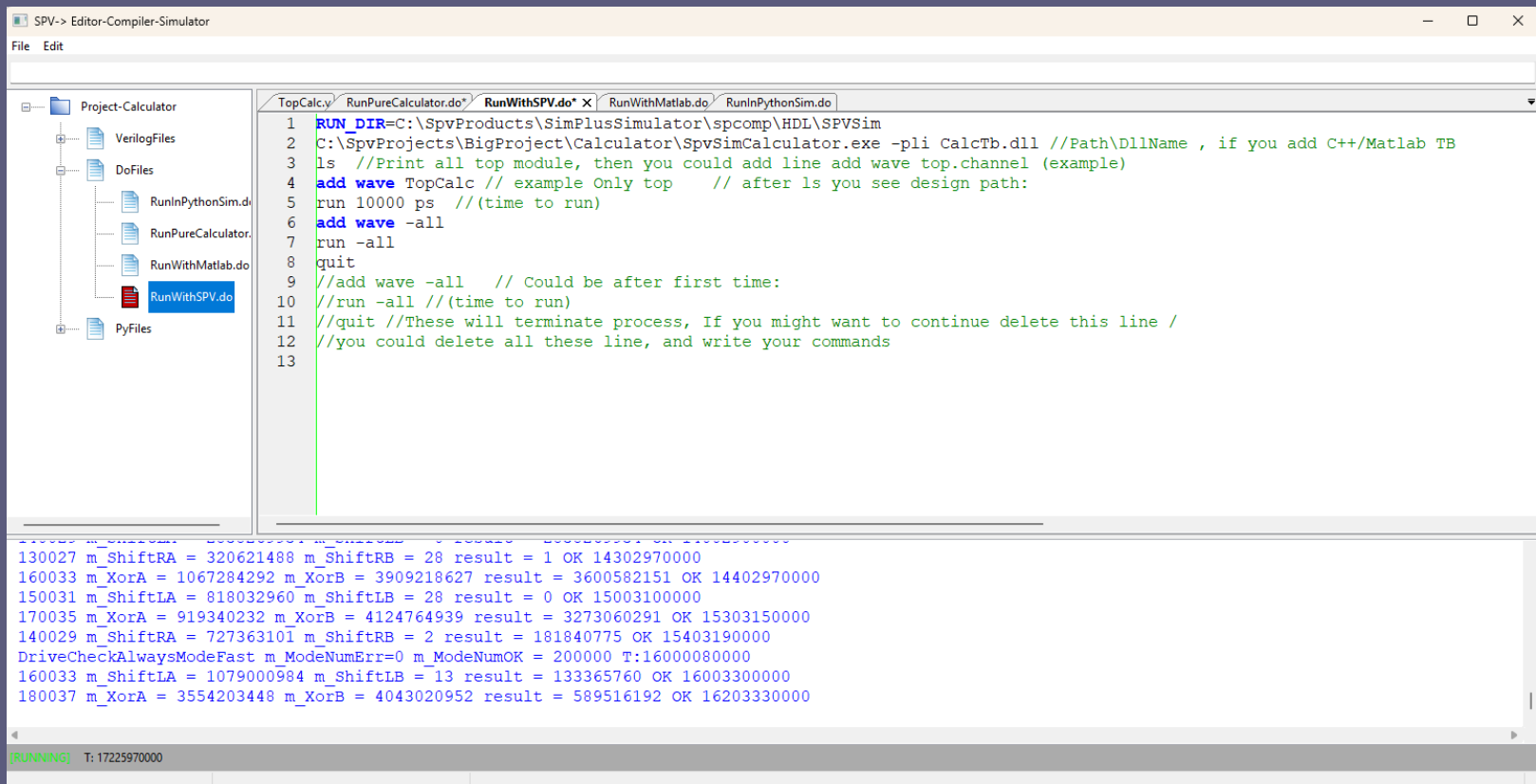


Testbench

SPV Verification $\Leftrightarrow$ Design



Unified Workspace for Code, Compilation Simulations, and Verification.



Scheduler and HDL interface Python

```
TopCalc.v RunPureCalculator.do* RunWithSPV.do* RunWithMatlab.do RunInPythonSim.do DriveOperand.py* X
1 #import SPSched
2 from SpvPython import *
3 from AllSig import *
4 import random
5 from random import randrange #, uniform
6 from datetime import datetime
7 from SPV import *
8
9 LoopSize = 80001;
10 def DriveAdd(id: int):
11     PR(threading.current_thread().name + " thread id = " + str(id) + " start at Time: " + str(SPV.SimTime()));
12     m_AddClkNeg = SPSigEvent(m_Sigclk_add,AtNeg);
13     GlobSched.WaitEv(m_AddClkNeg);
14     numOk=0;numErr=0;
15     for ActionInd in range (0,LoopSize):
16         GlobSched.WaitEv(m_AddClkNeg);
17         #GlobSched.WaitTime(40);
18         if (ActionInd > 0) :
19             resHdl = (m_Sigadd_res.Val32())&0xFFFFFFFF;
20             if (res != resHdl):
21                 PR("DriveAdd: Error at ind " + str(ActionInd) + " adda = " + str(adda) + " addb=" + str(addb) + " res="
22                 numErr = numErr+1;
23             else:
24                 numOk = numOk+1;
25             adda = SPV.Gen()%0x6FFFFFFF;
26             addb = SPV.Gen()%0x6FFFFFFF;
27             res = (adda + addb)&0xFFFFFFFF;#Expected
28             m_Sigadd_a.Set(adda);
29             m_Sigadd_b.Set(addb);
30             PR("DriveAdd: numErr=" + str(numErr) + " numOk=" + str(numOk));
31
32 def DriveSub(id: int):
33     import pdb; pdb.set_trace();
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```

Scheduler and HDL interface C++

```
// C++ version same performance as Verilog, but easier to read
cout << " DO_FAST_PROC=FALSE Mode loopSize = " << loopSize << endl;
StartTProc(this, (SpvProcMethod)&Driver::DriveCheckAlwaysOrTP);
StartTProc(this, (SpvProcMethod)&Driver::DriveCheckAlwaysAddTP);
StartTProc(this, (SpvProcMethod)&Driver::DriveCheckAlwaysSubTP);
StartTProc(this, (SpvProcMethod)&Driver::DriveCheckAlwaysMultTP);
StartTProc(this, (SpvProcMethod)&Driver::DriveCheckAlwaysAndTP);
```

```
void Driver::DriveCheckAlwaysAddTP()
{
    for (unsigned i = 0; i < loopSize; i++) {
        if (i) {
            Wait(m_ClkAddNeg);
            if (m_AddRes != SH::m_Sigadd_res) {
                cout << i << ": Error ***: m_AddA = 0x" << hex << m_AddA << " m_AddB = 0x" << m_AddB << " SPV result = 0x" << m_AddRes
                m_AddNumErr++;
            }
            else {
                m_AddNumOK++;
            }
        }
        m_AddA = GenUnsigned(); m_AddB = GenUnsigned(); m_AddRes = m_AddA + m_AddB;
        SH::m_Sigadd_a = m_AddA; SH::m_Sigadd_b = m_AddB;
    }
    cout << "DriveCheckAlwaysAddTP m_AddNumErr=" << m_AddNumErr << " m_AddNumOK = " << m_AddNumOK << endl;
}
```

Scheduler and HDL interface MATLAB

```
bool MatCalcInf::PrepareAddVector(vector<unsigned>& a, vector<unsigned>& b, vector<unsigned>& results, unsigned numObj)
{
    m_MLNumObj[0] = numObj;
    m_MLResults.Destroy();
    bool isOk = mlfPrepareListAdd(1, m_MLResults, m_MLNumObj);
    if (!isOk) return false;
    return PrepareData(a, b, results, numObj);
}
```

```
void Driver::DriveCheckAlwaysOrFast()
{
    static unsigned cnt = 0, ind = 0;
    if (cnt == 0) m_MatCalcInf->PrepareOrVector(m_OrAVec, m_OrBVec, m_OrResVec, m_VecSize);

    if (cnt++) {
        if (m_OrResVec[ind] != SH::m_Sigor_res) {
            cout << cnt << ": Error ***: m_OrA = 0x" << hex << m_OrAVec[ind] << " m_OrB = 0x" << m_OrBVec[ind] << " SPV result = 0x"
            m_OrNumErr++;
        } else {
            m_OrNumOK++;
        }
        if (++ind == m_VecSize) {
            m_MatCalcInf->PrepareOrVector(m_OrAVec, m_OrBVec, m_OrResVec, m_VecSize);
            ind = 0;
        }
    }
    //Set data and calculate expected for next negedge.
    SH::m_Sigor_a = m_OrAVec[ind]; SH::m_Sigor_b = m_OrBVec[ind];
    if (cnt > loopSize) {
        CurrAProc()->Kill();
        cout << "DriveCheckAlwaysOr m_OrNumErr=" << m_OrNumErr << " m_OrNumOK = " << m_OrNumOK << endl;
    }
}
```

Visual Interface: Test Editor and Regression Manager

Spv General Gui Tools Release 28/4/2020

Runtime Control Save tree Control Tests Control Create Tests Ctrl

MacFrame

Spv Test Runner

Spv Packet Tree

Spv Tests Editor

Spv Verilog Gui Stub

CurrTestDir.xml Test1 Default HdlConnection MacFrame

GROUP: CONTROL_EVENT

GROUP: CLOCK

GROUP: GENERAL

Comment: STOP_SIM: STOP1 WriteCover

TOGGLE_SIG: TOG_RST TOP_0::main_rst

GROUP: E1T2

GROUP: ALWAYS

GROUP: COVERAGE

GROUP: OTHER-FRAME

G_CONST: TYPE_A 8 0XFF

G_CONST: TYPE_B 8 0XAA

G_PERCENT: TYPE_VAL 8 {TY

PACKET: NESTED_A {A}

PACKET: NESTED_B {B}

PACKET: TEST {A,B,C,D,E,F,TYPE,FILE_FIELD,Nested-A,Nested-B}

GROUP: GB

GROUP: MATLAB

INIT_SIG: INIT_SIG 10 true 1

Create a packet, include sub packet

Entry-Name	KEY-NAME	COMMENT
PACKET:	TEST	

Packet field declaration

Field	Gen	Meth	Crc	End	Del	Add
A	☒	☐	☐	☐	☐	☐
B	☒	☐	☐	☐	☐	☐
C	☒	☐	☐	☐	☐	☐
D	☒	☐	☐	☐	☐	☐
E	☒	☐	☐	☐	☐	☐
F	☒	☐	☐	☐	☐	☐
TYPE	☒	☐	☐	☐	☐	☐
FILE_FIELD	☐	☐	☐	☐	☐	☐
Nested-A	☒	☐	☐	☐	☐	☐
Nested-B	☒	☐	☐	☐	☐	☐

SAVE CLOSE

IP Wiz

Data Obj

Generators

In Design Drive

CLI Commands

Generators

Communications

Packets

Coverage

Free Code

Visual Interface: Test Editor and Regression Manager

Spv General Gui Tools Release 28/4/2020

Spv Test Runner

Spv Packet Tree

Spv Tests Editor

Spv Verilog Gui Stub

Edit Runtime proj Regression test control ---Now Clock--- Hours/Minutes/Regression_policy

23 16 46 00 00 OnceNow

Regression test(Dir list)

- ☒ Runtime
 - ☐ Ethernity
 - ☐ NO_AES_ENCRYPT
 - ☒ Regression
 - ☒ aliveTest
 - ☐ bw
 - ☐ destroy
 - ☐ hash_tbl
 - ☒ hlend
 - ☒ hlnd_correct
 - ☒ hlnd_err_correctable
 - ☒ hlnd_err_uncorrectable
 - ☐ if
 - ☐ if_fec
 - ☐ if_hlnd_prsr
 - ☐ if_scrambler
 - ☐ if_tx_mac
 - ☐ interrupts
 - ☐ interrupts_set_and_clear
 - ☐ interrupt_dsync
 - ☐ interrupt_lods
 - ☐ interrupt_status_bits
 - ☐ omci_14
 - ☒ ploam
 - ☒ ploam_counters
 - ☒ ploam_queues
 - ☒ ploam_queues_almost_overflow
 - ☒ ploam_queues_overflow
 - ☒ ploam_queues_underflow
 - ☒ read_apb2_cs_ploam_regs
 - ☒ write_apb2_cs_ploam_regs
 - ☐ registers
 - ☒ sync
 - ☒ shifts
 - ☒ shift_0
 - ☒ shift_1
 - ☒ shift_62
 - ☒ shift_63
 - ☒ shift_rnd
 - ☐ tod
 - ☐ tx_mac
 - ☐ xmem

Test Log

```
Exec name is : C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe
work dir is : C:/SpvProjects/BigProject/Calculator/SPVSim
Command Args : -R -pli CalcTb.dll
total button are 8
Start running test : Regression/Test100000
Process C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe -R -pli CalcTb.dll launched
Run post command: copy spv.log "C:/SpvProjects/BigProject/Calculator/SPVSim/Runtime/Regression/Test100000"
Start running test : Regression/Test200000
Process C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe -R -pli CalcTb.dll launched
Run post command: copy spv.log "C:/SpvProjects/BigProject/Calculator/SPVSim/Runtime/Regression/Test200000"
Start running test : Regression/Test300000
Process C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe -R -pli CalcTb.dll launched
Run post command: copy spv.log "C:/SpvProjects/BigProject/Calculator/SPVSim/Runtime/Regression/Test300000"
Start running test : Regression/Test400000
Process C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe -R -pli CalcTb.dll launched
Run post command: copy spv.log "C:/SpvProjects/BigProject/Calculator/SPVSim/Runtime/Regression/Test400000"
Start running test : Regression/Test500000
Process C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe -R -pli CalcTb.dll launched
Run post command: copy spv.log "C:/SpvProjects/BigProject/Calculator/SPVSim/Runtime/Regression/Test500000"
Start running test : Regression/Test600000
Process C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe -R -pli CalcTb.dll launched
Run post command: copy spv.log "C:/SpvProjects/BigProject/Calculator/SPVSim/Runtime/Regression/Test600000"
Start running test : Regression/Test700000
Process C:/SpvProjects/BigProject/Calculator/SpvSimCalculator.exe -R -pli CalcTb.dll launched
Run post command: copy spv.log "C:/SpvProjects/BigProject/Calculator/SPVSim/Runtime/Regression/Test700000"
Finish running all simulation
----- The End -----
```

C:\SpvProjects\BigProject\Cal x + v

```
580117 m_ShiftRA = 319019621 m_ShiftRB = 10 result = 311542 OK 6
640129 m_ShiftLA = 3865143183 m_ShiftLB = 19 result = 101449728
```

Debug C++

Debug Python

```

129 void Driver::DriveCheckAlwaysOrFast()
130 {
131     static unsigned cnt = 0;
132     if (cnt++) {
133         if (m_OrRes != SH::m_Sigor_res) {
134             cout << cnt << ": Error ***: m_OrA = 0x" << hex << m_OrA << " m_OrB = 0x" << m_OrB << " SPV result = 0x" << m_OrRes << " HDL m_Sigor_res
135             m_OrNumErr++;
136         }
137         else {
138             m_OrNumOK++;
139         }
140     }
141     //Set data and calculate expected for next negedge.
142     m_OrA = GenUnsigned(); m_OrB = GenUnsigned(); m_OrRes = m_OrA | m_OrB;
143     SH::m_Sigor_a = m_OrA; SH::m_Sigor_b = m_OrB;
144     if (cnt > loopSize) {
145         CurrAProc()->Kill();
146         cout << "DriveCheckAlwaysOr m_OrNumErr=" << m_OrNumErr << " m_OrNumOK = " << m_OrNumOK << " T:" << SimTime() << endl;
147     }
148 }

```

119% No issues found Ln: 143 Ch: 15 Col: 18

Watch 1

Search (Ctrl+E) Search Depth: 3

Name	Value	Type
SimTime()	30000	const unsigned __int64 &
SH::m_Sigor_a	(my_Name="TopCalc.or_a" pSim_Type=0x0000023533cde470 (mIsSigExist=true my_Father=0x00007fffc1dc6f30 (CalcTbDB.dllSpvSig SH::m_Sigor_a) {...}) ...)	SpvSig
SpvMonitor	(m_IsSig=true)	SpvMonitor
my_Name	"TopCalc.or_a"	std::string
pSim_Type	0x0000023533cde470 (mIsSigExist=true my_Father=0x00007fffc1dc6f30 (CalcTbDB.dllSpvSig SH::m_Sigor_a) {...}) ...)	spv_Sim_Type *
m_Uval	0x0000023533cde498 (0)	unsigned int *
m_64Val	0x0000023533cde498 (0)	unsigned __int64 *
m_Size	32	unsigned int

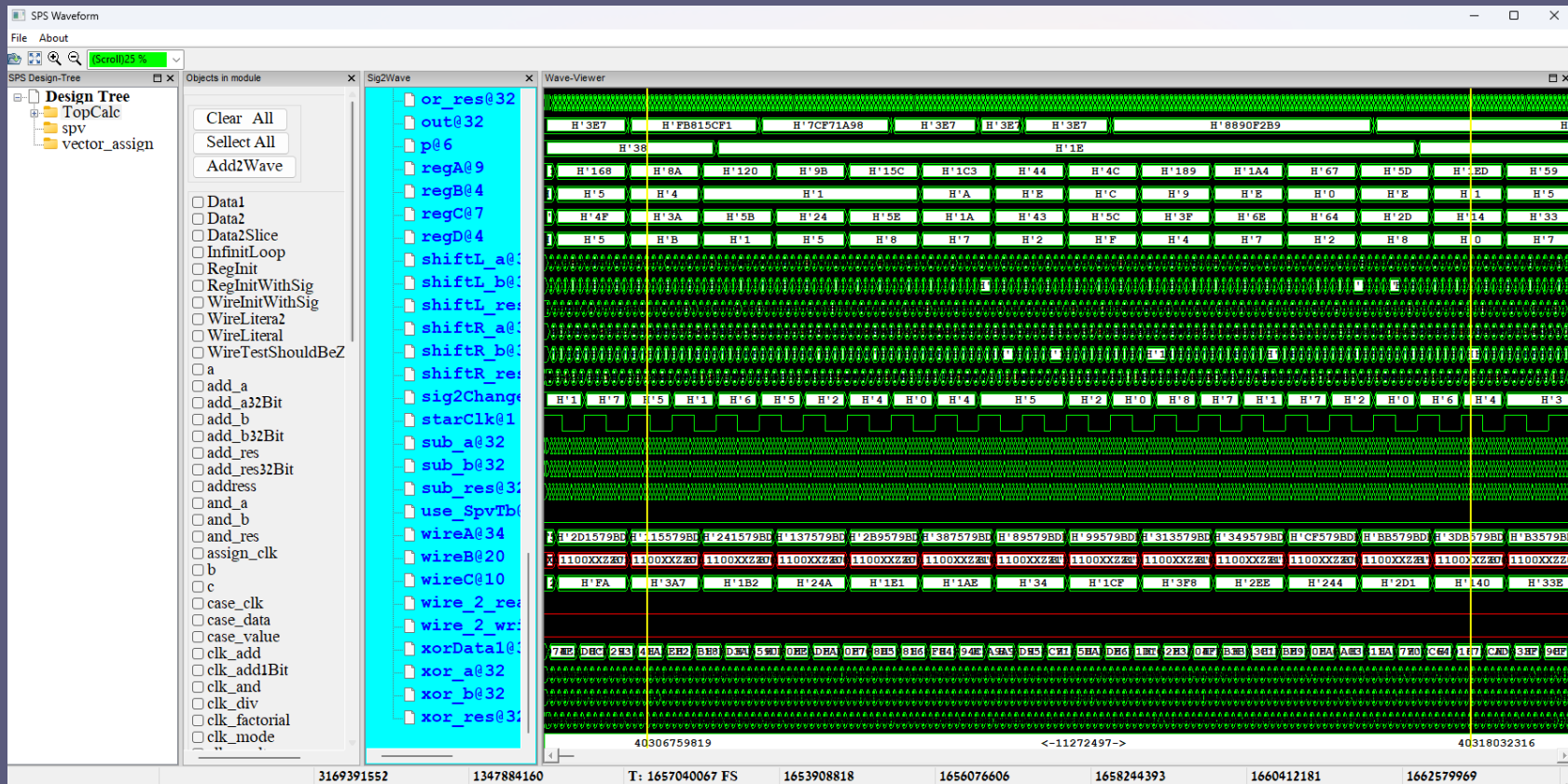
Output Watch 1

```

> c:\spvprojects\demoldir\pysim\driver.py(25)StartDrive()
-> for ActionInd in range (0,LoopSize):
(Pdb) n
> c:\spvprojects\demoldir\pysim\driver.py(26)StartDrive()
-> genVal = SPV.Gen();
(Pdb) n
> c:\spvprojects\demoldir\pysim\driver.py(27)StartDrive()
-> m_Sigbusa.Set(genVal);
(Pdb) p genVal
1003066593
(Pdb) p LoopSize
10000
(Pdb) |

```

Wave viewer





The End Thanks
